

Description

METHOD FOR FORMING A SELF-ALIGNED LTPS TFT

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method for forming a low temperature polysilicon thin film transistor (LTPS TFT), and more particularly, to a method for forming a self-aligned LTPS TFT.

[0003] 2. Description of the Prior Art

[0004] A liquid crystal display is broadly applied to portable electronic apparatuses, such as notebooks and personal digital assistants (PDAs), because of its thin display panel, low power consumption, and low-radiation. As the requirements of high quality displays increase, flat panels with high quality and low price are demanding in the future. An LTPS TFT, which is an actively driving TFT, is one of the important technologies for achieving the goal.

[0005] An LTPS TFT-LCD includes at least a transparent substrate, a pixel array region, a scan line driving circuit region, and a data line driving circuit region. The pixel array region comprises a plurality of parallel scan lines, a plurality of parallel data lines, and a liquid crystal molecule layer. Each scan line and each data line define a pixel, and each pixel further comprises a TFT and a storage capacitor. Current LTPS TFT-LCD integrates a standard driving IC in a liquid crystal panel by utilizing LTPS CMOS TFT technologies, thus the size of displays and the cost are reduced.

[0006] As shown in Figs.1-5, the schematic diagrams demonstrate a method for forming a top gate LPTS CMOS TFT 38 according to the prior art. As shown in Fig.1, the LTPS CMOS TFT 38 of the prior art comprises an N type low temperature polysilicon thin film transistor (NLTPS TFT) 34 and a P type low temperature polysilicon thin film transistor (PLTPS TFT) 36. The LTPS CMOS TFT 38 of the prior art is formed on a glass substrate 10, and the glass substrate 10 surface comprises a first region I for forming the NLTPS TFT 34, and a second region II for forming the PLTPS TFT 36. In addition, the glass substrate 10 surface further comprises a pixel array region (not shown in Fig.

1) for forming a plurality of NLTPS TFTs 34, which are used to be switches of pixel cells of an LCD, arranged in an array.

[0007] According to the prior art, an amorphous silicon (α -Si) layer (not shown in Fig.1) is formed on the substrate 10, and an annealing process is performed such that the amorphous silicon layer will be recrystallized to a polysilicon layer (not shown in Fig.1). Then, a first photo-etching process (PEP) is performed to form a patterned polysilicon layer 12 in both the first region I and the second region II of the substrate 10. Afterward, a low temperature deposition process is performed to form a gate insulating (GI) layer 14 to cover the patterned polysilicon layer 12 on the substrate 10, and an aluminum layer (not shown in Fig.1) is formed over the gate insulating layer 14. Finally, a second photo-etching process is performed to respectively form a gate electrode 16 of the NLTPS TFT 34 and the PLTPS TFT 36 in the aluminum layer of the first region I and the second region II.

[0008] As shown in Fig.2, an implantation process 18 is performed by utilizing the gate electrodes 16 as a mask to implant phosphorous ions into the patterned polysilicon layer 12, which is not covered by the gate electrode 16, to

form a plurality of N type lightly doped areas 20. As shown in Fig.3, a photo resist layer (not shown in Fig.3) is formed on the substrate 10, and a third photo-etching process is performed to form a patterned photo resist layer 22 in the photo resist layer to cover the second region II and the gate electrode 16 of the first region I. Then, an implantation process 24 is performed to implant arsenic ions into the patterned polysilicon layer 12, which is not covered by the patterned photo resist layer 22, to form two N type heavily doped areas 26s and 26d. The N type heavily doped areas 26s and 26d are for respectively being a source electrode and a drain electrode of the NLTPS TFT 34, the lightly doped areas 20, which are located on the side of the N type heavily doped areas 26s and 26d, are used to be lightly doped drains (LDD) of the NLTPS TFT 34, and the patterned undoped polysilicon layer 12, which is below the gate electrode 16 of the NLTPS TFT 34, is for being a channel area of the NLTPS TFT 34.

[0009] As shown in Fig.4, the remaining patterned photo resist layer 22 is removed, and another photo resist layer (not shown in Fig.4) is formed on the substrate 10. Then, a fourth photo-etching process is performed to form a pat-

terned photo resist layer 28 in the photo resist layer. Afterward, an implantation process 30 is performed by utilizing the patterned photo resist layer 28 and the gate electrode 16 of the PLTPS TFT 36 as a mask to implant boron ions into the patterned polysilicon layer 12, which is not covered by the photo resist layer 28 and the gate electrode 16, such that two P type heavily doped areas 32s and 32d for respectively being a source electrode and a drain electrode of the PLTPS TFT 36 are formed. The patterned undoped polysilicon layer 12, which is below the gate electrode 16, is used to be a channel area of the PLTPS TFT 36. Finally, as shown in Fig.5, the remaining patterned photo resist layer 28 is removed to form the NLTPS TFT 34 and the PLTPS TFT 36 of the LTPS CMOS TFT 38 of the prior art.

[0010] According to the method for forming the LTPS CMOS TFT 38 of the prior art, the gate electrodes 16 of the NLTPS TFT 34 and the PLTPS TFT 36 are first formed, than the N type lightly doped drains 20, the N type source electrode and drain electrode, and the P type source electrode and drain electrode are respectively formed.

[0011] Although the above-mentioned method utilizes the gate electrodes 16 as a self-aligned mask to form the N type

lightly doped areas 20, another photo resist mask is still required when forming the source electrode and the drain electrode of the NLTPS TFT 34. However, when defining the pattern of the photo resist mask in a photo process by a stepper or a scanner, misalignment or overlap could occur because of human or non-human factors. For example, as shown in Fig.3, the patterned photo resist layer 22 may shift left, and parts of the patterned polysilicon layer 25 will not be doped. Thus the lightly doped areas 20 will not be equally doped. The asymmetric lightly doped areas 20 not only are incapable of restraining the hot electron effect, but may also generate leakage current of the gate electrode, and further result in breakdown.

[0012] Therefore, to form a lightly doped drain with uniform width and avoid a too narrow range between the source electrode and the drain electrode resulting from the misalignment in the photo process is an important topic for study during the LTPS TFT manufacturing processes.

SUMMARY OF INVENTION

[0013] It is therefore one object of the present invention to provide a method for forming an LTPS TFT that can self align the lightly doped drains, the source electrode, and the drain electrode, such that the error resulting from the

photo process can be avoided.

[0014] It is another object of the present invention to provide a method for forming an LTPS CMOS TFT in a self-aligned manner to obtain symmetric lightly doped drains without superfluous processes.

[0015] According to the present invention, a method for forming an LTPS TFT on a substrate in a dual self-aligned manner is provided. The substrate surface comprises at least a first region for forming at least an NLTPS TFT, and at least a second region for forming at least a PLTPS TFT. First, a patterned undoped polysilicon layer is formed on each of the first and second regions of the substrate, and each patterned undoped polysilicon layer comprises a source area, a drain area, and a channel area. Then a dielectric layer and a patterned conductive layer are formed on the substrate to cover the patterned undoped polysilicon layer. The patterned conductive layer of the first region comprises two first gaps. Afterward, a first implantation process is performed to implant N type dopants into the source area and the drain area in the patterned undoped polysilicon layer by the first gaps in a self-aligned manner, such that an N type source electrode and an N type drain electrode are respectively formed. Thereafter, a cer-

tain width of the patterned conductive layer is removed to form two second gaps in the patterned conductive layer, and simultaneously a gate electrode of the N type LTPS TFT is defined. Subsequently, a second implantation process is performed to implant N type dopants into the patterned undoped polysilicon layer of the first region by the two second gaps in a self-aligned manner, such that two N type lightly doped drains (LDD) are formed. After, a gate electrode of the P type LTPS TFT is formed in the patterned conductive layer of the second region. Finally, a P type source electrode and a P type drain electrode of the P type LTPS TFT are formed in the source area and the drain area of the second region.

[0016] The present invention first utilizes the patterned conductive layer as a self-aligned mask to form the N type source and the N type drain, then utilizes the reduced patterned conductive layer as a self-aligned mask to form the N type lightly doped drain and the gate electrode, and finally utilizes the gate electrode as a self-aligned mask to form the P type source and the P type drain. The present invention utilizes multiple self-aligned processes to form the LTPS TFT, which does not increase superfluous processes and excessive costs, but obtains symmetric N type lightly

doped drains. Furthermore, the misalignment problem due to multiple photo-etching processes can be avoided.

[0017] These and other objects of the present invention will be apparent to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0018] Figs.1–5 are schematic diagrams of a method of forming an LTPS CMOS TFT according to the prior art.

[0019] Figs.6–14 are schematic diagrams of a method for forming an LTPS CMOS TFT according to a preferred embodiment of the present invention.

[0020] Figs.15–21 are schematic diagrams of a method for forming an LTPS CMOS TFT according to a second embodiment of the present invention.

DETAILED DESCRIPTION

[0021] The present invention provides a method for simultaneously forming an NLTPS TFT and a PLTPS TFT. However, the application of the present invention is not limited by the embodiments. In a preferred embodiment of the present invention, the method of the present invention

can be also applied to form an LTPS CMOS TFT composed of an NLTPS TFT and a PLTPS TFT. The LTPS CMOS TFT, NLTPS TFT, or PLTPS TFT of the present invention is formed in a periphery circuit area of an LCD for being a logic device. Moreover, the NLTPS TFT used to be a switching device could also be formed by the method of the present invention in a pixel array area of the LCD.

[0022] An example of forming an LTPS CMOS TFT 74 is used here for illustrating the method of the present invention.

Figs.6–14 are schematic diagrams of a method for forming the LTPS CMOS TFT 74 according to a preferred embodiment of the present invention. As shown in Fig.6, the LTPS CMOS TFT 74 is formed on a substrate 40, and the substrate 40 surface comprises an NLTPS TFT region III for forming an NLTPS TFT 70 and a PLTPS TFT region IV for forming a PLTPS TFT 72. The substrate 40 is a transparent insulating substrate, such as a glass substrate or a quartz substrate.

[0023] First, a sputtering process is performed to form an amorphous silicon layer (not shown in Fig.6 and Fig.7), having thickness between 400 to 600Å, on the substrate 40. Then, an annealing process, such as an excimer laser annealing (ELA) process, is performed to recrystallize the

amorphous silicon layer to a polysilicon layer (not shown in Fig.6). Afterward, a first photo-etching process is performed to form a patterned polysilicon layer 42 in both the NLTPS TFT region III and the PLTPS TFT region IV of the substrate 40. Each patterned polysilicon layer 42 comprises a source area, a drain area, and a channel area (all not shown in Fig.6). It is noted that the annealing process can be alternatively performed after the first photo-etching process. Additionally, a buffer layer (not shown in Fig.6) can be further formed between the substrate 40 and the amorphous silicon layer to prevent the substrate 40 from being damaged during the annealing process or the photo-etching process.

[0024] Following that, a low temperature deposition process is performed to form a silicon oxide layer or a silicon nitride layer, having thickness between 600 to 800Å, to cover the patterned polysilicon layer 42 on the substrate 40 as a gate insulating layer 44. Then a conductive layer 46 and a photo resist layer (not shown in Fig.6) are formed on the gate insulating layer 44. After, a second photo-etching process is performed. During the second photo-etching process, first a patterned photo resist layer 48 is formed, and then the conductive layer 46, which is not covered by

the patterned photo resist layer 48, is removed to form two gaps 50 in the conductive layer 46 as shown in Fig.7. Thereafter, an implantation process 52 is performed to implant N type dopants into the source area and the drain area in the patterned polysilicon layer 42 by the gaps 50 in a self-aligned manner, such that a source electrode 54s and a drain electrode 54d of the NLTPS TFT 70 are formed. It is noted that, the material of the conductive layer comprises aluminum, wolfram, chromium, or molybdenum, the dopant concentration in the implantation process is about $1\text{E}14$ to $1\text{E}16$ atoms/cm², and the N type dopants comprise arsenic or phosphorous.

[0025] As shown in Fig. 8 and Fig. 9, a trimming process is performed to reduce a certain width L of the patterned photo resist layer 48. Then an etching process is performed to remove the conductive layer 46 that is not covered by the reduced patterned photo resist layer 55, such that the width of the two gaps 50 will be enlarged to two larger gaps 56, and meanwhile a gate electrode 58 of the NLTPS TFT 70 is defined. After, an implantation process 60 is performed to implant N type dopants into the patterned polysilicon layer 42 by the two gaps 56 in a self-aligned manner, such that two N type lightly doped drains 60 are

formed. The trimming process includes an ash process, a descum process, and an ultraviolet beaming process or a thermal curing process. The dopant concentration in the implantation process is preferably about $1\text{E}12$ to $1\text{E}14$ atoms/cm², and the N type dopants comprise arsenic or phosphorous.

[0026] As shown in Figs. 10–12, a photo resist layer (not shown) is formed on the substrate 40 after removing the reduced patterned photo resist layer 54. Then, a third photo-etching process is performed. During the third photo-etching process, a patterned photo resist layer 62 is first formed to cover the gate electrode 58 of the NLTPS TFT 70 and the channel area of the PLTPS TFT region IV, then the conductive layer 46, which is not covered by the patterned photo resist layer 62, is removed to form a gate electrode 64 of the PLTPS TFT 72. The patterned photo resist layer 62 is used to define the gate electrode 64 of the PLTPS TFT 72 and to protect the gate electrode 58 of the NLTPS TFT 70, and the patterned photo resist only needs to cover the gate electrode 64 of the NLTPS TFT 72. Since the gate electrode 64 is well protected, a tiny alignment error is tolerable during the photo process.

[0027] As shown in Fig. 13 and Fig. 14, a photo resist layer (not

shown) is formed on the substrate 40 after removing the remaining patterned photo resist layer 62. Then a fourth photo-etching process is performed to form a patterned photo resist layer 66 in the photo resist layer. After, an implantation process 68 is performed to implant P type dopants into the source area and the drain area in the patterned polysilicon layer 42, which are not covered by the patterned photo resist layer 62 and the gate electrode 64, to form a source electrode 70s and a drain electrode 70d of the PLTPS TFT 72. Finally, the patterned photo resist layer 66 is removed to form the NLTPS TFT 70 and the PLTPS TFT 72 of the present invention. It is noted that the dopant concentration in the implantation process is preferably about $1\text{E}14$ to $1\text{E}16$ atoms/cm², and the P type dopants comprise boron or boron fluoride (BF₂).

[0028] Figs.15–21 are schematic diagrams of a method for forming an LTPS CMOS TFT 120 according to a second embodiment of the present invention. As shown in Fig.15, the LTPS CMOS TFT 120 is formed on a substrate 80, and the substrate 80 surface comprises an NLTPS TFT region V for forming an NLTPS TFT 114 and a PLTPS TFT region VI for forming a PLTPS TFT 116. First, a polysilicon layer (not shown in Fig.15) is formed on the substrate 80, then a

first photo-etching process is performed to form a patterned polysilicon layer 82 in both the NLTPS TFT region V and the PLTPS TFT region VI, and a gate insulating layer 84, a conductive layer 86, and a photo resist layer 88 are sequentially formed on the substrate 80.

[0029] As shown in Fig.16 and Fig.17, a second photo-etching process is performed to form two gaps 90 in the photo resist layer 88, and an isotropic etching process, such as a wet etching process, is performed to remove the conductive layer 86 that is not covered by the photo resist layer 88, such that two gaps 92 are formed in the conductive layer 86 (the width of the gaps 92 is larger than that of the gaps 90), and a gate electrode 94 of the NLTPS TFT 114 is simultaneously defined. Then, an N type implantation process 96 is performed by utilizing the photo resist layer 88 as a mask to form two N type heavily doped areas 98s and 98d in the patterned polysilicon layer 82. After, the photo resist layer 88 is removed, and an N type implantation 100 is performed by utilizing the gate electrode 94 and the conductive layer 86 as a mask to form a plurality of N type lightly doped areas 102 and 104 in the patterned polysilicon layer 82 of the NLTPS TFT region V. The N type heavily doped areas 98s and 98d are respec-

tively used to be a source electrode and a drain electrode of the NLTPS TFT 114, the N type lightly doped areas 102 are used to be lightly doped drains of the NLTPS TFT 114, and the patterned undoped polysilicon layer 82 below the gate electrode 94 of the NLTPS TFT 114 is used to be a channel area of the NLTPS TFT 114.

[0030] As shown in Fig.18 and Fig.19, a photo resist layer (not shown in Fig.18) is formed on the substrate 80, and a third photo-etching process is performed to form a patterned photo resist layer 104 in the photo resist layer. Then, the conductive layer 86, which is not covered by the patterned photo resist layer 104, is removed to form a gate electrode 106 of the PLTPS TFT 116. Afterward, an implantation process 108 is performed by utilizing the patterned photo resist layer 104 as a mask to respectively form two P type heavily doped areas 110s and 110d in the source area and the drain area of the PLTPS TFT region VI for respectively being a source electrode and a drain electrode of the PLTPS TFT 116.

[0031] As shown in Figs.20 and 21, a fourth photo-etching process is performed after removing the remaining patterned photo resist layer 104. During the fourth photo-etching process, a patterned photo resist layer 112 is first formed

on the substrate 80 to cover the gate electrode 104 and the gate electrode 106 of the PLTPS TFT 116, and then the conductive layer 86, which is not covered by the patterned photo resist layer 112, is removed. Finally, the patterned photo resist layer 112 is removed to form the NLTPS TFT 114 and the PLTPS TFT 116 of the LTPS CMOS TFT 120 of the present invention.

[0032] While it is one object of the present invention to form a top gate LTPS CMOS TFT, the application of the present invention is not limited by the embodiments. The present invention can also be applied to form scan lines, data lines, and storage capacitors of an LTPS TFT-LCD, and other low temperature polysilicon thin film transistors. Furthermore, an NLTPS TFT can be formed according to the method shown in Figs.6-10 in the preferred embodiment, while a PLTPS TFT can be alternatively formed according to the method shown in Figs.11-14 according to the second embodiment of the present invention, and vice versa.

[0033] According to the method for forming an LTPS CMOS TFT of the present invention, a patterned conductive is used as a self-aligned mask to form an N type source electrode and an N type drain electrode, the reduced patterned con-

ductive layer is used as a self-aligned mask to form N type lightly doped drains, then a gate electrode is formed, and finally the gate electrode is used as a self-aligned mask to form a P type source electrode and a P type drain electrode. The present invention utilizes multiple self-aligned processes to form the LTPS CMOS TFT without increasing superfluous processes, which not only reduce the costs but also obtain symmetric N type lightly doped drains. Further the misalignment problem resulting from multiple photo-etching processes can be avoided.

[0034] In contrast to the prior art, though the present invention utilizes four photo-etching processes as the prior art does, the present invention utilizes multiple self-aligned processes to form the source electrode, the drain electrode, and the lightly doped drains. Therefore, the NLTPS TFT and the PLTPS TFT of the present invention are more reliable, and further the misalignment problem can be avoided. It is worth noticing that the method of the present invention can be not only applied to form the NLTPS TFT and the PLTPS TFT, but also applied to form LTPS CMOS TFT.

[0035] Those skilled in the art will readily appreciate that numerous modifications and alterations of the device may be

made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.